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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/443,160	11/19/1999	DAVID L. ISAMAN	98-MET-069	6854

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STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/443,160	ISAMAN, DAVID L.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-21* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Clams 2-21 are presented for examination. Claim 1 has been canceled.

In view of the Appeal Brief filed on 11/19/07, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Hesson (5,666,506).

3. As to claim 2, 12, Hesson taught at least:
A pipelined microprocessor (see pipeline processor in col.1, lines 29-34 for background) capable of detecting an instruction that loads data from a first memory location that was previously stored to (see comparison of instruction in col.4, lines 64-67, col.5, lines 1-13) .

4. Hesson did not explicitly show the instruction is detected without requiring computation of an external memory address as claimed. However, Hesson taught comparison of the virtual address (see col.4, lines 65-67). Examiner holds that virtual address is not external, and the comparison is not computation. Therefore, Hesson is without address computation.

5. As to Claims 3,13, Hesson taught detecting an instruction that stores data into a second memory location that was previously read from without computing an external memory address of said second memory location (see store address being compared to all load addresses in col.6, lines 35-41).

6. As to claims 4, 14, Hesson was also applicable for detecting instructions that load data from identical memory locations that were previously stored to (see col.6, lines 35-42). As to the feature of without computing external memory addresses, see discussions in Paragraph 4 above.

7. As to claims 5,15, Hesson also taught detecting instructions that store data into identical memory locations that were previously read from (see the load were

allowed to proceed after store violation in col.6, lines 13-15).

8. As to claims 6,7, 16,17, Hesson's virtual addresses were symbolic structure (see virtual address in col.4, lines 64-67).

9. As to claim 8, 9, 18,19, examiner holds that virtual same address must have identical base and identical offset.

10. As to claim 10, 11, Hesson also taught a bypass element [violation condition] capable of sending a bypass signal to an instruction execution stage of pipelined microprocessor that indicates that instructions referred to an identical memory location (see store violation condition detected in col.6, lines 35-42).

11. As to claims 20, Hesson also taught at least :

12.

a) detecting a first instruction that stores data to a first memory location, said first instruction comprising syntax (see virtual address comparison) for computing an effective address for the first memory location and the operands needed to compute the effective address in (see the store instruction for the first instruction in store barrier hit detection in col.5, lines 3-13, see the virtual addresses as the syntax);

b) detecting a second instruction that loads data from a second memory location, the second instruction comprising syntax for computing an effective address for said second memory location (see the snoop of the load instruction as the second instruction in col.6, lines 13-21).

13. Hesson did not explicitly show the determination of syntax relationship between the first memory location and said second memory location, without computing the effective address for said first memory location and without computing the effective

address for the second memory location as clamed. However, Hesson, in the same patent, taught already comparison of virtual addresses of the load instruction and store instruction conflicts (see col.4, lines 56-67, col.5, lines 1-13). Examiner holds that virtual address comparison is not computation. Therefore, Hesson is without address computation.

14. As to the detection of the instructions, examiner holds that for the purpose of detecting the load/store conflicts, Hesson must detect the op code of an instruction to see whether it was a load or store instruction, and virtual addresses by the instructions must comprise a syntax for computing effective address of memory location.

15. As to claim 21, Hesson was also directed to identical memory location (see the address conflicts in col.6, lines 3-29).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Ameson et al. (5,475,823) is cited for the teaching of detection circuit [520] detecting the load instruction accessing a location previously stored (see fig.5, 4, lines 55-67, col.8, lines 10-24, lines 37-48);

b) Kiyohara et al. (5,694,577) is cited for the teaching of comparison of virtual addresses of preload instructions and store instructions (see col.2, lines 55-65, col.5, lines 49-61);

c) Ball (5,615,357) is cited for disclosure of a system including a determination of syntax relationship (see the model of CPU) without itself calculating effective addresses of the first a and second instructions (see the trace file containing the load and store instruction effective addresses in col.2, lines 39-45, lines 64-67, col.3, lines 1-

6, col.4, lines 1-11, col.11, lines 59-67, see col.10, lines 10-52 for the trace driven mode, see col.12, lines 1-7 for load and store).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

D. PAN
PRIMARY EXAMINER
ART UNIT

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100